IN THE CLAIMS:

The text of all pending claims is set forth below. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (Previously Presented) An information processing unit, comprising:

a prefetch buffer prefetching an instruction through a bus with its width being at least twice as large as an instruction length, to store the prefetched instruction;

a decoder decoding the instruction stored in said prefetch buffer;

an arithmetic unit executing the decoded instruction;

an instruction request control circuit performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch instructions; and

a prefetch control circuit prefetching the branch target instruction to said prefetch buffer when a branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

2. (Original) The information processing unit according to claim 1, wherein said prefetch buffer prefetches the instruction from a main memory through an instruction cache memory.

3. (Previously Presented) The information processing unit according to claim 2, wherein said prefetch control circuit outputs to the instruction cache memory a control signal canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent an access to the main memory, the access being caused by a cache miss.

4. (Original) The information processing unit according to claim 2, wherein said prefetch buffer prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length, and outputs the instruction to said decoder through a bus with its width equal to the instruction length.

5. (Original) The information processing unit according to claim 4, wherein said prefetch buffer stores four pieces of instructions at maximum.

6. (Original) The information processing unit according to claim 1, wherein said decoder and said arithmetic unit perform operations in units of one instruction.

7. (Original) The information processing unit according to claim 1, wherein said instruction request control circuit and said prefetch control circuit perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

8. (Original) The information processing unit according to claim 1, wherein the branch instruction includes a conditional branch instruction and/or an unconditional branch instruction.

9. (Previously Presented) The information processing unit according to claim 1, further comprising a register writing therein an execution result of said arithmetic unit.

10. (Previously Presented) An information processing method, comprising:

prefetching an instruction through a bus with its width being at least twice as large as an instruction length, to store the prefetched instruction;

decoding the prefetched instruction;

executing the decoded instruction;

performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch instructions; and

prefetching the branch target instruction when a branch is ensured to occur by executing the branch instruction, while ignoring the branch target instruction when a branch does not occur.

11. (Previously Presented) The information processing method according to claim 10, wherein said prefetching an instruction prefetches the instruction from the main memory from an instruction cache memory.

12. (Previously Presented) The information processing method according to claim 11, wherein said prefetching the branch target instruction outputs to the instruction cache memory a control signal canceling the prefetch request, which has been performed to prefetch the branch target instruction, when the branch does not occur, to thereby prevent the access to the main memory, the access being caused by a cache miss.

13. (Previously Presented) The information processing method according to claim 11, wherein said prefetching an instruction prefetches the instruction from the instruction cache memory through a bus with its width being twice as large as an instruction length, and outputs the instruction to said decoding through a bus with its width equal to the instruction length.

14. (Previously Presented) The information processing method according to claim 13, wherein said prefetching an instruction stores 4 pieces of instructions at maximum.

15. (Previously Presented) The information processing method according to claim 10, wherein said decoding and said executing perform operations in units of one instruction.

16. (Previously Presented) The information processing method according to claim 10, wherein said performing a prefetch request and said prefetching the branch target instruction perform operations to allow, when a delayed branch instruction appears, a branch to occur following an instruction subsequent to the delayed branch instruction.

17. (Original) The information processing method according to claim 10, wherein said branch instruction includes a conditional branch and/or an unconditional branch.

18. (Original) The information processing method according to claim 10, wherein said execution step writes an execution result to a register.

19. (Previously Presented) An information processing method, comprising:

prefetching an instruction through a bus with a width at least twice as large as the length of the instruction, and storing the prefetched instruction;

performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch instructions; and

prefetching the branch target instruction when a branch is ensured to occur by executing the branch instruction, and ignoring the branch target instruction when a branch does not occur.

20. (Currently Amended) An information processing apparatus, comprising:

means for prefetching and storing an instruction through a bus with a width at least twice as large as the length of the instruction;

means for performing a prefetch request to prefetch a branch target instruction when a branch instruction is decoded, otherwise performing the prefetch request sequentially to prefetch instructions;

means for prefetching the branch target instruction when a branch is ensured to occur by executing the branch instruction[[;]], and ~~means for~~ ignoring the branch target instruction when a branch does not occur.